REMARKS

INTRODUCTION:

In accordance with the foregoing, claim 3 has been amended, and claim 6 has been added. No new matter is being presented, and approval and entry are respectfully requested.

Claims 3, 4, 5 and 6 are pending and under consideration. Reconsideration is respectfully requested.

ENTRY OF RESPONSE UNDER 37 C.F.R. §1.116:

Applicants request entry of this Rule 116 Response and Request for Reconsideration because:

(a) it is believed that the amendment of claims 3 and 4 and the addition of claim 6 put this application into condition for allowance as suggested by the Examiner;

(b) the amendments were not earlier presented because the Applicants believed in good faith that the cited prior art did not disclose the present invention as previously claimed;

(c) the amendments of claims 3 and 4 and addition of claim 6 should not entail any further search by the Examiner since no new features are being added or no new issues are being raised; and/or

(d) the amendments do not significantly alter the scope of the claims and place the application at least into a better form for appeal. No new features or new issues are being raised.

The Manual of Patent Examining Procedures sets forth in §714.12 that "[a]ny amendment that would place the case either in condition for allowance or in better form for appeal may be entered." (Underlining added for emphasis) Moreover, §714.13 sets forth that "[t]he Proposed Amendment should be given sufficient consideration to determine whether the claims are in condition for allowance and/or whether the issues on appeal are simplified." The Manual of Patent Examining Procedures further articulates that the reason for any non-entry should be explained expressly in the Advisory Action.

REJECTION UNDER 35 U.S.C. §102:

In the Office Action, at pages 2-3, numbered paragraph 4, claim 3 was rejected under 35 U.S.C. §102(b) as being anticipated by Nakata et al. (USPN 5,825,193; hereafter, Nakata). This rejection is traversed and reconsideration is requested.

It is respectfully submitted that Nakata recites a device for determining a count of a

number of semiconductor elements that would be unsatisfactory in a burn-in step, but does not recite a burn-in operation. That is the device of Nakata is a semiconductor integrated circuit having a self-test circuit formed on the semiconductor substrate, together with a failure counting circuit formed on the semiconductor substrate to count the number of times the self-test circuit provides a failure signal. The device may further include a frequency multiplying circuit formed on the semiconductor device to provide the self-test circuit a reference signal whose frequency is a multiple of the clock signal's frequency. In addition, the device may have a burn-in control voltage circuit formed on the semiconductor device to maintain a constant reference voltage inputted to the burn-in voltage control circuit. Thus, Nakata recites providing high accuracy synchronizing signals to individual SICs and conducts on-wafer circuit testing with the aid of a self-test circuit on the substrate to avoid wasting burn-in time by predetermining whether an SIC device is satisfactory, as noted in col. 3, lines 1-4, of Nakata:

> As a result of such arrangement, the frequency of external signals can be reduced and, at the same time, it becomes possible to apply a high-frequency reference signal to a self-test circuit. Therefore, it is possible to reduce the ill-influence from external environments as well as to determine whether an SIC element works properly by a high-speed, high-accuracy synchronizing signal. The first object is accomplished accordingly. (emphasis added)

and col. 3, lines 40-44:

> As a result of such arrangement, all SICs are fed the same voltage, regardless of their on-wafer locations. Without the influence from, for example, a drop in voltage, individual SIC devices can be subjected to an on-wafer circuit testing process or to a burn-in process at the same time. (emphasis added)

Thus, Nakata recites an on-wafer testing process and a burn-in process utilizing elements on the semiconductor substrate, in contrast to the present invention, which utilizes a burn-in tank, in which the semiconductor device is placed for testing, wherein a converter that is not located on the semiconductor substrate is used for the burn-in process.

Claim 3 has been amended to recite, in part, a converter that is added at the output of the signal generator and located outside of a substrate supporting the semiconductor device, which is not recited by Nakata et al., which only utilizes burn-in elements located on the substrate supporting the semiconductor.

Thus, claim 3 is submitted not to be anticipated under 35 U.S.C. §102(b) by Nakata et al. (USPN 5,825,193).

ALLOWABLE SUBJECT MATTER:

Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if suitably rewritten.

Claim 3 has been amended, and is now submitted to be in allowable form. Since claim 4 depends from amended claim 3, claim 4 is submitted to be allowable for at least the reasons that amended claim 3 is submitted to be allowable.

Claim 5 is allowed over the art of the record.

NEW CLAIM:

New claim 6 recites that the features of the present invention include a dynamic burn-in apparatus for a semiconductor device, wherein a signal output from a signal generator is provided to a semiconductor device to be tested in a burn-in tank, comprising: a converter arranged at the output of the signal generator and outside of a substrate supporting the semiconductor device, wherein the converter increases, by N times, N a positive integer, a frequency of the signal output from the signal generator and outputs the signal having the increased frequency to the semiconductor device to be tested in the burn-in tank to implement expedited dynamic burn-in, increasing a rate of detection of defects due to initial deterioration.

Nothing in the prior art teaches or suggests such. It is submitted that this new claim distinguishes over the prior art.

CONCLUSION:

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot, and further, that all pending claims patentably distinguish over the prior art. Thus, there being no further outstanding objections or rejections, the application is submitted as being in condition for allowance which action is earnestly solicited. At a minimum, this Amendment should be entered at least for purposes of Appeal as it either clarifies and/or narrows the issues for consideration by the Board.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited and possibly concluded by the Examiner contacting the undersigned attorney for a telephone interview to discuss any such remaining issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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